REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

The Examiner objects to the Abstract containing reference numerals and referring to a particular figure. By this amendment, the Abstract has been amended to remove those reference numerals and the figure identification. Withdrawal of the objection to the Abstract are respectfully requested.

Claims 16 and 25 stand objected to under CFR §1.75(c) as allegedly being in improper dependent form and failing to further limit the subject matter of a previous claim. Particularly, the Examiner contends that claim 15 already recites "the execution of instructions to control processing, instructions that inherently reside on some sort of computer readable medium (computer program product). Therefore, because there is no way that the processing of instructions of claim 15 can function as claimed without the instructions being comprised on the computer program product, claim 16 fails to further limit the subject matter of claim 15." This objection is respectfully traversed.

Claim 15 is a method claim, and it specifically recites steps for processing data. As a method claim, it is not limited to a particular apparatus or other structure. In particular, it is not limited to being used in conjunction with a computer program product. For example, the method steps could be implemented in a computer or other data processor whose memory stores program instruction. Nor is a computer or data processor the same thing as computer program product. Claim 16 is different from claim 15 because it is not a method claim. It is an apparatus claim specifically directed to a computer program product. A computer program user that actually implements the method steps of claim 15 may not make or sell computer program products that store that computer program. On the other hand, a software manufacture may not sell computers,

but instead may only sell computer program products that store computer programs that control a computer. Such a manufacturer may not be directly infringing a method claim, although it could be indirectly infringing the claim. But that manufacturer would be directly infringing claim 17 assuming that the sold product included a computer program for controlling a computer to perform the method of claim 16.

Thus, the Examiner's characterization of claim 17 is incorrect. First, it is not a method claim, but rather an apparatus claim. Second, it does define something different from the method claim as explained above. Third, the Examiner's attention is directed to a recently issued U.S. Patent 6,795,841 which includes a method claim 1 for "processing input data words." Claim 15 recites "a computer program including a computer program for controlling a data processing apparatus to perform data processing in accordance with the method as claimed in claim 1." This is just one example of many in which the U.S. PTO has properly issued this type of claim. Withdrawal of the objection to claims 16 and 25 is therefore respectfully requested.

Claims 1-22 stand objected because of several informalities. Regarding the informalities noted in subparagraphs 9(a) - 9(c), the Examiner's suggestions have been adopted. Regarding the objections and dependencies with respect to claims 9-16, claim 12 now depends from 11, and claim 16 now refers back to the method of claim 15. Withdrawal of the objections to the claims is respectfully requested.

Claims 1-16, and 22 stand rejected under 35 CFR §112, second paragraph as allegedly being indefinite. The examiner objects to the clause "a plurality of operations that may be specified by instructions" in claims 1, 15 and 22. These claims have been amended to delete the words "that may," which Applicants believe overcomes the Examiner's concern.

Claim 3 is objected to by the Examiner indicating that it is unclear whether "match signals" refers to a separate group of signals. Claim 3 has been amended to substitute "are the same as" for the word "match," which is believed to overcome the Examiner's objection.

By correctly referring to the method of claim 15, the Examiner's objection to claim 16 is also overcome.

Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

Claims 1-8, 10, 13, and 15 and 16 stand rejected 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,909,567 to Novak et al. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Novak fails to satisfy this rigorous standard.

Novak discloses in Figure 2 a block diagram of a processor 120. Main memory supplies two types of instructions for two respective operating modes. In a complex instruction set computer (CISC) instruction operating mode, main memory 130 supplies CISC-type instructions to predecoder 270 and instruction decoder 220. The instruction decoder 220 converts CISC instructions into operations of a reduced instruction set computer (RISC) architecture instruction set. In a native operating mode, the main memory supplies native mode RISC operations to a native Op supply circuit 224. The native mode Op supply circuit 224 serves as a by-pass path

for passing RISC operations directly to the RISC processor core when native mode operations are enabled.

Novak fails to disclose a "processor core having an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set that are to executed are fetched from a memory and along which instructions progress" and an instruction translator "within said instruction pipeline." The Examiner refers to Figures 2 and 5 and to column 2, lines 55-56. It is clear from Figure 2, and from the text in columns 3 and 4 that describes, it CISC instructions and RISC instructions are not both fetched and then passed through the same pipeline within which the decoder is situated. To the contrary, CISC instructions are fetched and passed along one path to the instruction decoder 220. See column 4, lines 11-16. On the other hand, RISC instructions follow another different path. As explained in column 4, lines 41-48, the

> native mode Op supply circuit 224 receives native mode RISC operations from the instruction cache 214 in the form of quad instruction." The quad instructions are loaded into the Op buffer 226 and the sequencing logic 228...transfers the four native mode RISC operations to the scheduler 260 **by a third path 239** in a single clock cycle. (emphasis added).

The instruction decoder 220 which translates between CISC instruction RISC instructions is not in the same path as the native Op buffer 226. Thus, Figure 2 and the related descriptive text explicitly describe two separate paths for the two different types of instructions

Claim 1 clearly defines the boundaries of the pipeline by specifying that the processor core has "an instruction pipeline into which instructions of said first instruction set and instructions of a second instruction set that are to be executed are fetched" and by reciting that the instruction translator is located in that same instruction pipeline. In contrast, Novak fetches

and translates CISC instructions separately from the native mode RISC instructions. The translated instructions are sent to the execution engine 222 in parallel with the native instructions but by different paths. Independent claims 15, 17 and 24 includes similar distinguishing features. Accordingly, the rejections based upon Novak should be withdrawn.

Claims 17-19, and 24-25 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,249,861 to Tremblay et al. This rejection is respectfully traversed.

Tremblay discloses an instruction fetch unit aligner for a non-power of two size instruction. Thus, Tremblay is not even concerned with translation from one instruction set to another instruction that occurs within a processor pipeline. Nevertheless, the Examiner alleges Tremblay discloses an instruction translator referencing the instructional aligner 308 contained in the instruction fetch unit 108.

Instructional aligner 308 does not translate instructions from one instruction set to those of another. Instead, aligner 308 aligns instructions of different lengths such that whole instructions can be stored in an instruction cache unit 106 rather than parts of instructions. Figure 2 referred to by the Examiner simply shows various formats of instructions having a non-power of two size. The alignment operation described by Tremblay in column 3, lines 10-24 referred to by the Examiner simply relates to efficiently fetching and storing at least two sequential cache lines "and then efficiently extracting and aligning all the bytes of a non-power of two size instruction from the line buffers." There is no translation described by Tremblay of one instruction set to another instruction set. Similar distinctions are found between claim 24 and Tremblay. The anticipation rejection based on Tremblay should therefore be withdrawn.

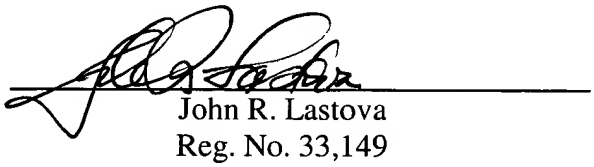
Claims 9, 11-12, and 14 stand rejected under 35 U.S.C. §103 as being unpatentable over Novak in view of U.S. Patent 5,898,885 to Dickol et al. Claim 20 stands rejected under 35

U.S.C. as being unpatentable over Tremblay in view of Dickol. Claims 21 and 22 stand rejected under 35 U.S.C. over Tremblay in view of Novak. These rejections are respectfully traversed because the rejections of the independent claims are improper and must be withdrawn.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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